Notice of Allowability	Application No.	Applicant(s)	
	10/757,227	DEWITT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 7/12/06*.

2. ☒ The allowed claim(s) is/are *1,3,5-11,13 and 15-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/19/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Francis Lammes on July 21, 2006.

The application has been amended as follows:

- Amend **claim 1** to read as follows:

1. A method of identifying false cache line sharing during execution of a computer program in a multiprocessor data processing system, comprising:

associating processor flag bits with at least one portion of a cache line in a cache, wherein the processor flag bits include a processor flag bit for each processor of the multiprocessor data processing system;

determining whether the cache line is being falsely shared between processors based on values of the processor flag bits; ~~and~~

modifying storage of a contents of the cache line to avoid false sharing of the cache line based on a determination that the cache line is being falsely shared between processors of the multiprocessor data processing system;

receiving an access request directed to a portion of the cache line; and

sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line.

- Cancel **claim 2**

- Amend **claim 3** as follows:

  Line 1: Replace "2" with --1--

- Cancel **claim 4**

- Amend **claim 11** to read as follows:

11. A computer program product in a recordable-type computer readable medium for identifying false cache line sharing during execution of a computer program in a multiprocessor data processing system, comprising:

first instructions for associating processor flag bits with at least one portion of a cache line in a cache, wherein the processor flag bits include a processor flag bit for each processor of the multiprocessor data processing system;

second instructions for determining whether the cache line is being falsely shared between processors based on values of the processor flag bits; ~~and~~

third instructions for modifying storage of a contents of the cache line to avoid false sharing of the cache line based on a determination that the cache line is being falsely shared between processors of the multiprocessor data processing system;

fourth instructions for receiving an access request directed to a portion of the cache line; and

fifth instructions for sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line.

- Cancel **claim 12**

- Amend **claim 13** as follows:

  Line 1: Replace "12" with --11--

- Cancel **claim 14**

- Amend **claim 21** to read as follows:

21. An apparatus for identifying false cache line sharing during execution of a computer program in a multiprocessor data processing system, comprising:

means for associating processor flag bits with at least one portion of a cache line in a cache, wherein the processor flag bits include a processor flag bit for each processor of the multiprocessor data processing system;

means for determining whether the cache line is being falsely shared between processors based on values of the processor flag bits;

means for modifying storage of a contents of the cache line to avoid false sharing of the cache line based on a determination that the cache line is being falsely shared between processors of the multiprocessor data processing system;

means for receiving an access request directed to a portion of the cache line; and

means for sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line.

Allowable Subject Matter

Claims 1, 3, 5-11, 13, and 15-21 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose the combination including the limitations of:

(**Claim 1**) "...sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line."

(**Claim 11**) "...fifth instructions for sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line."

(**Claim 21**) "...means for sending an interrupt to an interrupt handler associated with a performance monitoring application in response to a determination that false cache line sharing between processors is present with regard to the cache line."

As dependent **claims 3, 5-10, 13, and 15-20** depend from an allowable base claim, they are at least allowable for the same reasons as noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
Art Unit 2185
July 21, 2006

Brian R. Peugh
Primary Examiner